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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,098	09/12/2003	Michael Stewart Lyons	544732000400	6580

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EXAMINER	
ABRAHAM, ESAW T	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,098	LYONS, MICHAEL STEWART	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *5-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *5-10* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election / Restriction

Restriction to one of the following invention is required under 35 U.S.C. 121

I. Claims 1-4 drawn to a method for accessing data comprising the acts of: receiving a block of words from an array of synchronous random access memory; addressing the array; initiating a first read burst from the array; iterating a transfer, the transfer comprising the acts of: reading a word of error-free data from the array, the word of data containing error detection read redundancy bits; confirming an absence of errors in the word of error-free data by performing an error detection algorithm upon the word; and placing a copy of the word of error-free data into a FIFO; reading a further word of data from the array; detecting a correctable error in the further word of data; terminating the first read burst; correcting the further word to form a corrected word; placing a first copy of the corrected word into the FIFO; writing a further copy of the corrected word into the array; initiating a second read burst from the array; and further iterating the transfer, whereby the request is honored classified in class 714/762.

II. Claims 5-10, drawn to a memory storage device controller comprising: a Read FVO; a Write FIFO; a Write back FIFO; a bidirectional port corrected to a synchronous RAM array, the synchronous RAM array operable to respond to commands; a multiplexer operable to supply data to the port; a command processor having an input operable to receive data from the Write FIFO, the command processor further operable to supply formatted RAM commands to the multiplexer; an encoder having an input operable to receive data from the Write FIFO and to supply encoded data to the multiplexer; an EDC (error detection and correction) block having an

input operable to receive data from the port and further having an output operable to supply data to the Read FIFO and Write back FIFO, the EDC block, the EDC block operable to correct correctable data error and to detect correctable data errors; and an address block controlled by the command processor, the address block operable to supply addresses to the multiplexer classified in 714/758.

The invention are distinct, each from the other because of the following reasons: Invention Group I and group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has a separate utility such as a method for accessing data comprising the acts of: receiving a block of words from an array of synchronous random access memory; addressing the array; initiating a first read burst from the array; iterating a transfer, the transfer comprising the acts of: reading a word of error-free data from the array, the word of data containing error detection read redundancy bits; confirming an absence of errors in the word of error-free data by performing an error detection algorithm upon the word; and placing a copy of the word of error-free data into a FIFO; reading a further word of data from the array; detecting a correctable error in the further word of data; terminating the first read burst; correcting the further word to form a corrected word; placing a first copy of the corrected word into the FIFO. In the instant case, invention Group II, has a separate utility such as a memory storage device controller comprising: a Read FIFO; a Write FIFO; a Write back FIFO; a bidirectional port corrected to a synchronous RAM array, the synchronous RAM array operable to respond to commands; a multiplexer operable to supply data to the port; a command processor having an input operable to receive data from the Write FIFO, the command processor

further operable to supply formatted RAM commands to the multiplexer; an encoder having an input operable to receive data from the Write FIFO and to supply encoded data to the multiplexer; an EDC (error detection and correction) block having an input operable to receive data from the port and further having an output operable to supply data to the Read FIFO and Write back FWO, the EDC block, the EDC block operable to correct correctable data error and to detect correctable data errors; and an address block controlled by the command processor, the address block operable to supply addresses to the multiplexer (see MPEP 806.05(d)).

Because these inventions are distinct for the reason given above and the search required for the group I is not required for group II, restricting for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and the search required for group II is not required for group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Norman R. Klivans on 01/03/06 a provisional election was made with traverse to prosecute the invention of group I claims 1-4.
The applicant in replying to this office action must make affirmation of this election.

Claims 5-10 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

DETAILED ACTION

1. Claims 1-4 remained for the examination. Applicant is reminded that the non-elected claims 5-10 are to be cancelled from the file on or at allowance.

Claim objections

2. Claim 1 is objected to because of the following informalities:

Please change the phrase "the word of data" to ---the word of error-free data--- (see claim 1 line 7).

Please change the phrase "further word " to ---further word of data--- (see claim 1 line 16).

Please define the full word of a written word or phrase for the **abbreviations** "FIFO" as specified in the specification (see page 2, paragraph 0010).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness

or nonobviousness.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raynham (U.S. PN: 6,418,068).

As per claim 1:

Raynham in figure 3 teach or disclosed a method of accessing synchronous dynamic random access memory (SDRAM) (300) includes controller (312), mode registers (316), refresh counter (318), address register (328) for addressing the SDRAM, address bus (330), write FIFO and drivers (350), input registers (352), and receivers (354) (see col. 6, lines 4-25). Further, Raynham teaches that READ and WRITE accesses to SDRAM (300) are burst oriented--accesses start at a selected location and continue for a programmed number of locations in a programmed sequence (see col. 8, lines 21-67). Furthermore, Data from any READ burst completed or truncated before a subsequent WRITE command can be issued and if truncation is necessary, the BURST TERMINATE command is used (col. 9, lines 22-30). Raynham **does not explicitly teach** confirming an absence of errors in the word of error-free data by performing detection algorithm. **However,** Raynham teaches memory configurations (see figure 3 elements 100A and 100B) include an ECC scheme that is used for burst error detection, allowing for correction of at least single bit errors after single bit or 4-bit nibble errors have occurred and the ECC scheme preferably provides correction for 1 bit soft errors during the scrubbing operation (discussed above with respect to FIGS. 2A-2C), after a 1 bit, or a 4-bit nibble, hard error has occurred (see col. 11, lines 42-50) which Raynham system is basically teaching the same thing when generating ECC for burst error detection meaning confirming an absence of errors and detecting a correctable errors. **Therefore,** it would have been obvious to a person having an

ordinary skill in the art at the time the invention was made to use ECC scheme used for burst error detection and correction for confirming error free data or detecting correctable error as taught by Raynham for detecting faults. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because confirming error-free data or detecting correctable error using ECC scheme used for burst detection/correction is well known futures of ECC devices.

As per claims 2 and 3:

Raynham teaches memory configurations (100A and 100B) include an ECC scheme that is used for burst error detection, allowing for correction of at least single bit errors after single bit or 4-bit nibble errors have occurred (see col. 11, lines 42-50).

As per claim 4:

Raynham teaches data from any READ burst completed or truncated before a subsequent WRITE command can be issued and if truncation is necessary, the BURST TERMINATE command is used (col. 9, lines 22-30).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 5,978,954 Ou et al.

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Esaw Abraham

Art unit: 2133

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